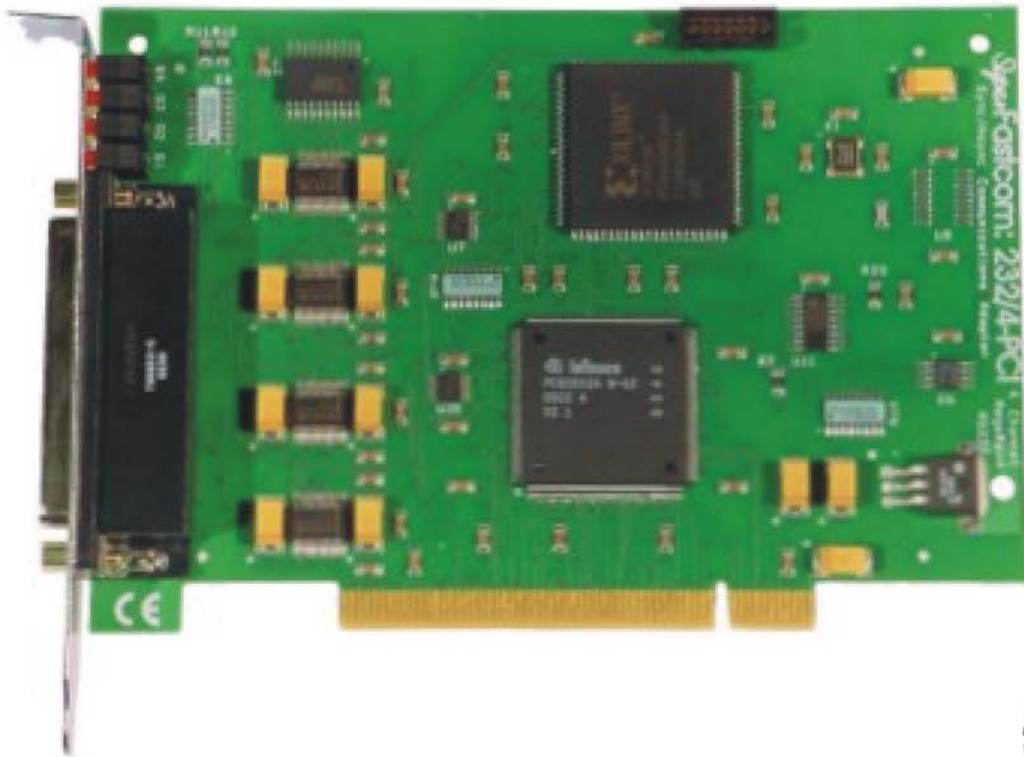


FASTCOM[®] ADAPTERS

SUPERFASTCOM 232/4-PCI

**Four Channel High Speed Synchronous Serial Interface
for PCI Bus**

Hardware Reference Manual



COMM-TECH, INC.

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REVISION NOTES

REVISION	PAGE NUMBER	CHANGES MADE
1.0	All	Document created
1.1	1	Added SuperFastcom family information
1.2	15	Changed warranty period to lifetime
1.3	11-12	Added more programs to list
1.4	16-17	Added "Errata" section Modified features to agree with errata
1.5	17	Appended to "Errata" section
1.6	10	Add hardware installation notes 2a & 2b
1.7	13	Added local bus register descriptions
1.8	19	Changed warranty to limited lifetime



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EUROPEAN UNION DECLARATION OF CONFORMITY Information Technology Equipment

The Company COMMTECH, INC. declares under its own and full responsibility that the product

" SuperFastcom 232/4-PCI - Revision 1.3 "

on which is attached this Certificate is compliant to the "89/336/EEC" Directive, amended by 92/31/EEC and 93/88/EEC.

[] The product identified above complies with the requirements of the above EU Directive by meeting the following standards:

- EN 50081-1 (1992) EMC Generic Emission Standard - Part 1, Residential, Commercial and Light Industry
 - EN 55022 (1995), CISPR 22 (1993) Limits and Methods of Measurement of Radio Disturbance Characteristics of Information Technology Equipment, 30 MHz - 1 GHz, Class B Limits
- EN 50082-1 (1992) EMC Generic Immunity Standard - Part 1, Residential, Commercial and Light Industry
 - IEC 801-2 (1984), Method of Evaluating Susceptibility to Electrostatic Discharge, Level 4
 - IEC 801-3 (1984), Radiated Electromagnetic field Requirements, Level 3
 - IEC 801-4 (1988), Electrical Fast Transient/Burst Requirements, Level 2

Products listed on this declaration are exempt from the requirements of the 73/23/EEC directive due to the input voltage specification as stated in Article 1 of the directive.

The technical documentation required to demonstrate that this product meets the requirements of the EMC Directive has been compiled by the signatory below and is available for inspection by the relevant enforcement authorities.

In WICHITA, KS on December 31st of 2002

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INTRODUCTION

The new *SuperFASTCOM 232/4-PCI* adapter is a high-speed, four-channel, synchronous serial communications adapter designed for Windows- and LINUX-based industrial/commercial systems. Its outstanding features include data rates up to 1 Mbps and the ability to buffer up to 4 Gigabytes of data (Windows 2000) in system memory.

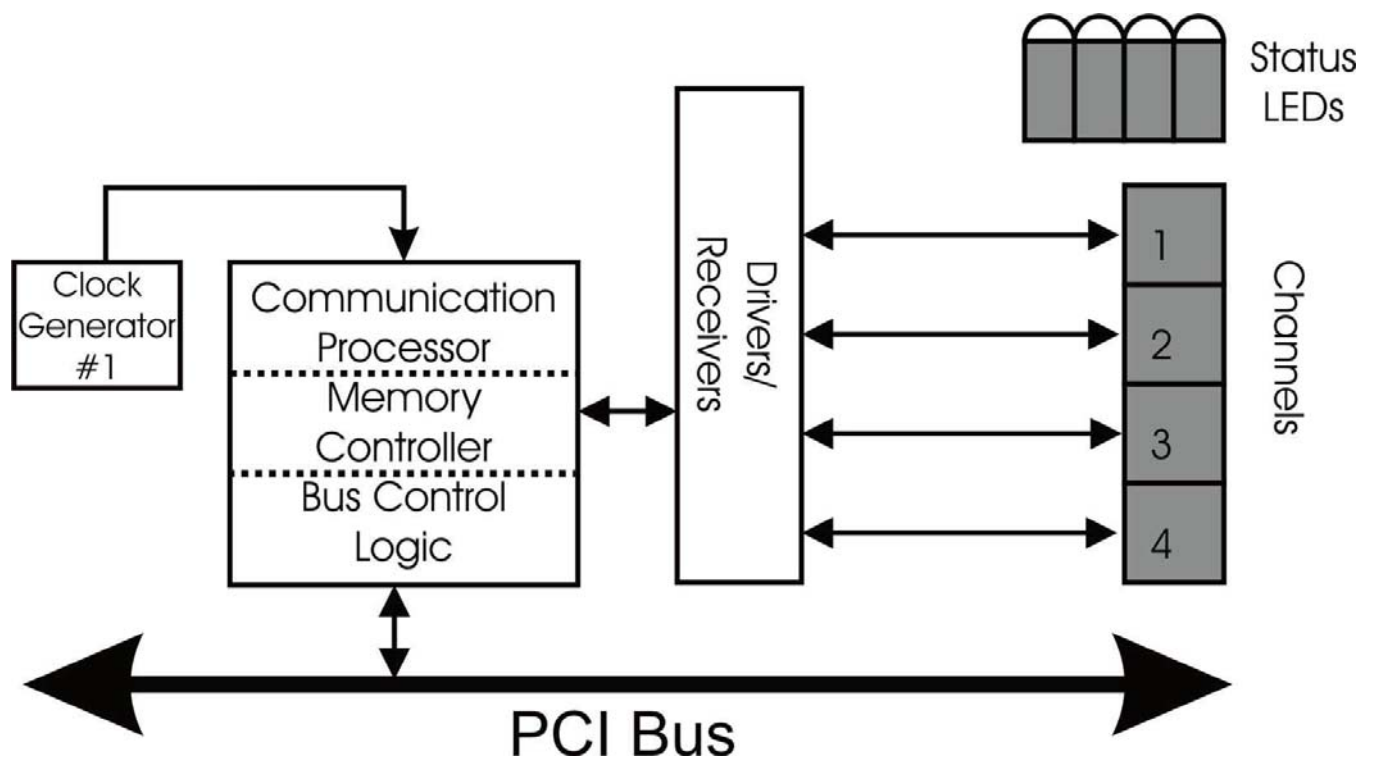
The *SuperFASTCOM 232/4-PCI* supports standard synchronous protocols (HDLC, SDLC) and their variations, as well as standard asynchronous data formats. The board features high-speed RS-232 drivers and receivers that allow all standard baud rates up to 921.6 Kbps, and can be easily set to operate at *any* non-standard baud rate (rates above 1 Mbps are possible but not guaranteed).

Programming is simplified with the inclusion of drivers, example programs and comprehensive documentation supplied on the Fastcom CD. The *SuperFASTCOM 232/4-PCI* provides high speed and high reliability while greatly reducing development time and system complexity.

The *SuperFASTCOM* family includes:

Form Factor	Line Type	Ports
PCI	RS422/485 OR RS232	4
PC/104+	RS422/485	1 or 2
CompactPCI	RS422/485	4
CompactPCI Rear IO	RS422/485	4

The following diagram illustrates the basic structure of the *SuperFASTCOM 232/4-PCI*:



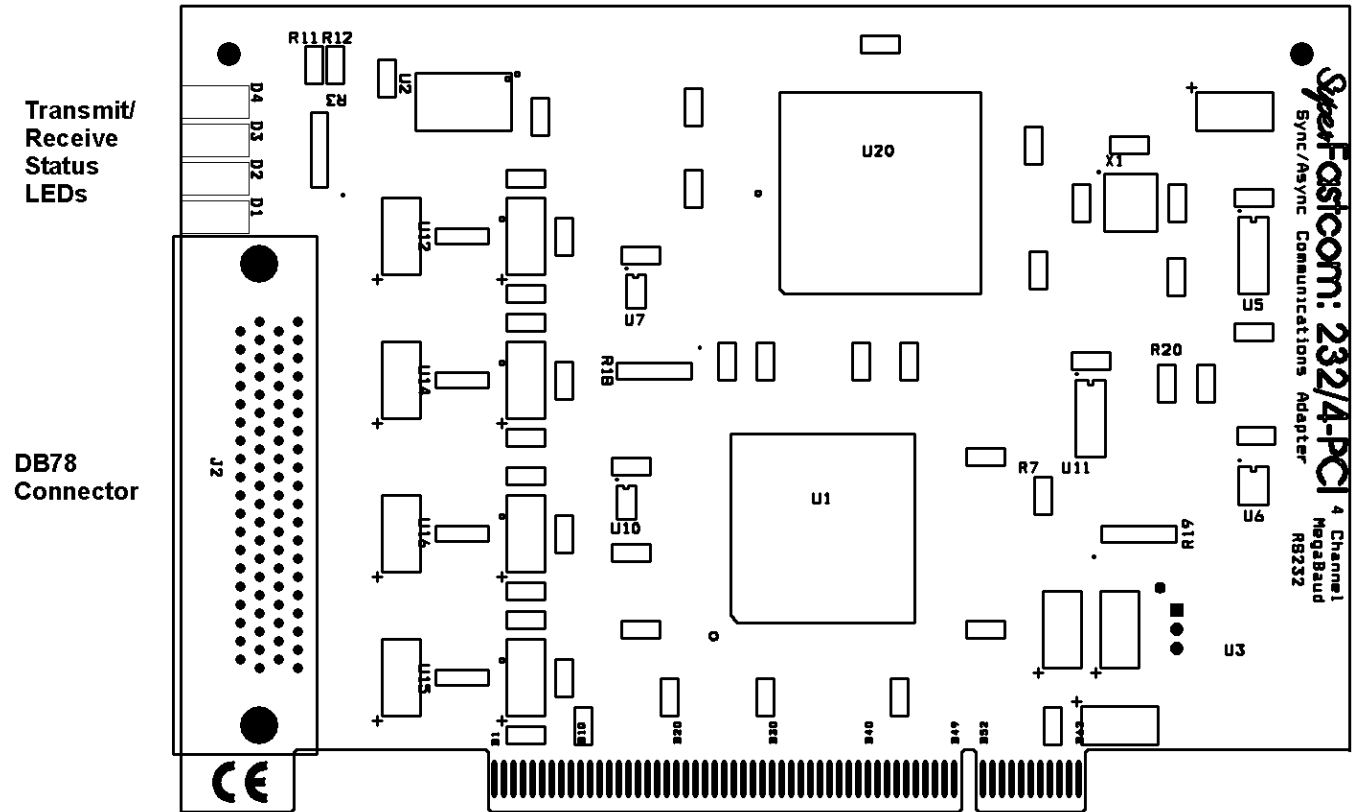
Specifications

Communications Controller:	Infineon 20534
OS Support:	Linux, Windows XP, 2000, NT4
Data Rate:	All baud rates up to and above 1Mbps (See Maximum Data Rate section)
Data Buffering:	Up to 4 GB (Windows)
Drivers/Receivers:	High Speed RS-232
Signals:	TxD, RxD, RTS, CTS, DCD, TT, RT, ST
Connector Configuration:	DB78 male to 4 DB25 male
Bus Interface:	32-bit PCI Ver. 2.1
Power Requirements:	450mA @ +5V (typical)
Environment	
Operating Temperature Range:	0°C to 70°C
Humidity:	0 to 90% (non-condensing)
Mean Time Between Failure:	24.61 Years
Certification:	FCC compliant, CE marked

Features

- **Four independent channels**
- **Status LEDs for system development/debugging**
- **Programmable on-board clock generator**
- **“Switchless” design for durability and reliability**
- **Durable Cables with RFI shielding**
- **Hardware documentation and software included on CD**
- **Made in Wichita, KS U.S.A.**

Board Layout



Status LEDs:

Red Transmit
Yellow Receive

PACKING LIST

SuperFASTCOM 232/4-PCI card
SuperFASTCOM 232/4-PCI cable assembly
Fastcom CD

If an omission has been made, please call technical support for a replacement.

COMMUNICATIONS OVERVIEW

- HDLC/SDLC Protocol Modes
 - Automatic flag detection and transmission
 - Shared opening and closing flag
 - Generation of inter-frame time fill '1's or flags
 - Detection of receive line status
 - Zero bit insertion and deletion
 - CRC generation and checking (CRC-CCITT or CRC-32)
 - Transparent CRC option per channel and/or per frame
 - Programmable Preamble (8 bit) with selectable repetition rate
 - Error detection (abort, long frame, CRC error, short frames)
- Bit Synchronous PPP Mode
 - Bit-oriented transmission of HDLC frame (flag, data, CRC, flag)
 - Zero bit insertion/deletion
 - 15 consecutive '1' bits aborts sequence
- Octet Synchronous PPP Mode
 - Octet-oriented transmission of HDLC frame (flag, data, CRC, flag)
 - Programmable character map of 32 hard-wired characters (00 H -1F H)
 - Four programmable characters for additional mapping
 - Insertion/deletion of control-escape character (7D H) for mapped characters
- Asynchronous (ASYNC) Protocol Mode
 - Selectable character length (5 to 8 bits)
 - Even, odd, forced or no parity generation/checking
 - 1 or 2 stop bits
 - Break detection/generation
 - In-band flow control by XON/XOFF
 - Immediate character insertion
 - Termination character detection for end of block identification
 - Time out detection
 - Error detection (parity error, framing error)
- BISYNC Protocol Mode
 - Programmable 6/8-bit SYN pattern (MONOSYNC)
 - Programmable 12/16-bit SYN pattern (BISYNC)
 - Selectable character length (5 to 8 bits)
 - Even, odd, forced or no parity generation/checking
 - Generation of inter-frame time fill '1's or SYN characters
 - CRC generation (CRC-16 or CRC-CCITT)
 - Transparent CRC option per channel and/or per frame
 - Programmable Preamble (8 bit) with selectable repetition rate
 - Termination character detection for end of block identification
 - Error detection (parity error, framing error)
- Extended Transparent Mode
 - Fully bit transparent (no framing, no bit manipulation)
 - Octet-aligned transmission and reception
- Protocol and Mode Independent
 - Data bit inversion
 - Data overflow and under run detection
 - Timer

Protocol Support

- Address Recognition Modes
 - Mode 0 - No address recognition
 - Mode 1 - 8-bit (high byte) address recognition
 - Non-Auto Mode - 8-bit (low byte) or 16-bit (high and low byte) address recognition

General

- On-chip Rx and Tx data buffer (the buffer size is 128 32-bit words each)
- Programmable transmit buffer size per channel; receive buffer allocation on request.
- Programmable watermark for receive channels to control transfer of receive data to host memory.
- Two programmable watermarks for each transmit channel, i.e. one controlling data loading from host memory and one controlling transfer of transmit data to the corresponding Serial Communication Controller (SCC).
- Internal test loop capability.

SuperFASTCOM 232/4-PCI / ESCC FAMILY COMPARISON

Enhancements to the ESCC Serial Core

The *SuperFASTCOM 232/4-PCI* adapter contains the core logic of the ESCC2 V3.2A as the heart of the device. Some enhancements are incorporated in the *SuperFASTCOM 232/4-PCI*. These are:

- 16-Kbyte packet length byte counter
- Enhanced address filtering (16-bit maskable)
- Enhanced time slot assigner
- Support of high data rates (1 Mbps). Protocol support is limited to HDLC Sub-modes without address recognition.

Simplifications of the ESCC Serial Core

The following features of the ESCC core have been removed:

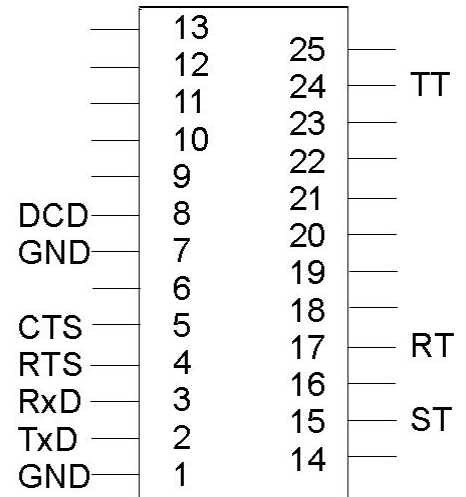
- SDLC Loop mode
- Extended transparent mode 0 (this mode provided octet buffered data reception without usage of FIFOs; the *SuperFASTCOM 232/4-PCI* supports octet buffered reception via appropriate threshold configurations for the SCC receive FIFOs)

CABLE CONFIGURATION

The cable provided with your *SuperFASTCOM 232/4-PCI* adapter splits each channel from the DB78 to into four DB 25 male connectors.

<u>SIGNAL</u>	<u>DB25 #</u>	<u>DB78 PIN NUMBER</u>			
		<u>CHANNEL 1</u>	<u>CHANNEL 2</u>	<u>CHANNEL 3</u>	<u>CHANNEL 4</u>
GND	1	58	38	9	48
GND	7	68	29	10	49
SD	2	70	13	22	62
RD	3	73	36	6	65
RTS	4	71	33	3	63
CTS	5	74	18	27	66
DCD	8	57	12	28	60
TT	24	52	11	21	47
RT	17	56	35	5	43
ST	15	55	15	24	44

DB25 CONNECTOR DESCRIPTION



Signal Pin Descriptions

<u>PIN#</u>	<u>NAME</u>	<u>DESCRIPTION</u>	<u>232 CIRCUIT</u>	<u>RS-232 DESCRIPTION</u>
1	GND	Ground	AA	Protective Ground
7	GND	Ground	AB	Signal Ground/Common Return
2	TxD	Transmit Data	BA	Transmitted Data
3	RxD	Receive Data	Bb	Receive Data
4	RTS	Request to Send	CA	Request to Send
5	CTS	Clear to Send	CB	Clear to Send

Clock Signal Pin Descriptions

<u>PIN#</u>	<u>NAME</u>	<u>DESCRIPTION</u>	<u>232 CIRCUIT</u>	<u>RS-232 DESCRIPTION</u>
8	DCD	Data Carrier Detect	CF	Received Line Signal Detector
24	TT	Transmit Clock Out	DA	Transmitter Signal Element Timing (DTE)
17	RT	Receive Clock In	DD	Receiver Signal Element Timing (DCE)
15	ST	Transmit Clock In	DB	Transmitter Signal Element Timing (DCE)

INSTALLATION

Hardware Installation

Important: Observe Electrostatic Discharge (ESD) precautions when handling the *SuperFASTCOM 232/4-PCI* board.

1. Remove the cover from your PC.
2. Unpack the *SuperFASTCOM 232/4-PCI* adapter. Keep the box and static bag for warranty/repair returns.
 - a. *The SuperFastcom requires that the selected PCI slot be capable of bus mastering. The card will not function correctly if installed into a non-bus mastering slot.*
 - b. *If possible, install the SuperFastcom into one of the Primary PCI slots. If you are installing into a Secondary PCI slot (i.e., on the other side of a PCI bridge), make sure that your motherboard's PCI bridge is properly installed in your operating system before proceeding with the installation. If you do not have more than three PCI slots, then none of the slots are secondary.*
3. Select an open PCI slot in your PC.
4. After removing the blank bracket from your PC, install the *SuperFASTCOM 232/4-PCI* in the PC by pressing it firmly into the slot. Install the bracket screw to hold it firmly in place.
5. Replace the cover on your PC.
6. Install the *SuperFASTCOM 232/4-PCI* cable.

Software Installation

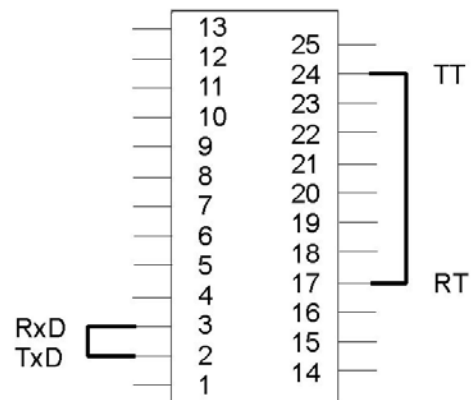
Select the link above to open the Installation Manual. Under *SuperFASTCOM*, select your operating system and follow the instructions. When you are finished, select *SuperFASTCOM 232/4-PCI* from the list at the end of the *SuperFASTCOM* section to return to this manual.

TESTING THE INSTALLATION

To fully test the installation of your *SuperFASTCOM 232/4-PCI*, you will need to build a "loop back plug". Materials needed are a DB25 female receptacle (solder cup style) and a few short pieces of 20 or 24 AWG stranded wire. Jumper the pins together on the DB25 as illustrated:

Windows 2000 Test Procedure

1. Place the loop back plug onto the Port 1 connector.
2. Open a console/DOS window.
3. Change directories to where you installed/copied the software.
4. Execute: `setclock 0 1000000`
5. Execute: `sfcset 0 hdlcset`
6. Execute: `loopback 0 h`



The red and yellow LEDs for port 1 should be blinking/on. Wait a few moments, press a key, and the errors/number of bytes sent through the loop will be displayed. The numbers will vary depending on how long you allow the test to run

The rest of the ports can be checked by executing:

- ⇒ sfcset 1 hdlcset
- ⇒ loopback 1 h

- ⇒ sfcset 2 hdlcset
- ⇒ loopback 2 h

- ⇒ sfcset 3 hdlcset
- ⇒ loopback 3 h

SOFTWARE UTILITIES

These programs and their source can be found on the Fastcom CD or downloaded from our website at <http://www.commtech-fastcom.com/>. They are meant to be used as educational tools and programming references when designing your own software.

- sfcset.exe Use to change register settings in conjunction with the hdlcset file
- hdlcset, asyncset, bisyncset
Generic settings files to be used with sfcset.exe
- getclock.exe returns programmable clock #1 rate (osc)
- getclock2.exe returns programmable clock #2 rate (progclk +/-)
- setclock.exe sets the programmable clock #1 (osc)
- setclock2.exe sets the programmable clock #2 (prograclk +/-)
- loopback.exe user program to effect a loopback on a SuperFastcom channel
- sfcmf.exe
 - Install your loopback plug onto the SuperFastcom.
 - Run "sfcmf.exe".
 - Select "connect" from the menu.
 - A dialog will open. Select the port to use (0,1,2,3).
 - Click on "OK".
 - An info box will open; click "OK".
 - Type a message: "Hello, world".
 - What you type should show up under "Transmit" in the window.
 - Select "Send" from the menu.
 - The message will appear in red under "Received".
 - To open a different port, either select "File->New" or "Disconnect" from the menu.
- readlb.exe user program to read a SuperFastcom special register
- writelb.exe user program to read a SuperFastcom special register
- readreg.exe user program to read a 20534 register
- writereg.exe user program to write to a 20534 register
- send.exe user program that opens a file and sends it through port 0

- flushrx.exe user program to flush the SuperFASTCOM receiver/buffers
- flushtx.exe user program to flush the SuperFASTCOM transmitter/buffers
- getbufs.exe user program to get buffering/descriptor parameters for a port
- setbufs.exe user program to set buffering/descriptor parameters for a port
- getclock.exe user program to get the current clock generator settings
- getclock2.exe user program to get the current program clock generator settings
- read_file_hdlc.exe user program to read hdlc frames from a port and stuff them to a file
- sendfile.exe user program to send a file out a SuperFastcom port
- setchecktimeout.exe user mode function to set the timeout timer in the driver that checks for frames to be returned or sent
- setfs6131clock.exe user program that sets the fs6131 clock generator which is only valid if you have an extended temperature card with fs6131's on it
- setrfi.exe user program to mask/unmask the frame end interrupt indication for receive descriptors
- setrirq.exe user program to set the interrupt rate for receive descriptors
- settirq.exe user program to set the interrupt rate for transmit descriptors
- settfi.exe user program to mask/unmask the frame end interrupt indication for transmit descriptors
- simuln200.exe user program to generate 26 byte hdlc frames simulating an LN200
- st_tt.exe user program to switch the onboard txclk multiplexer between the TT output and the ST input
- status.exe user program to read status from a SuperFastcom port

PROGRAMMING

Refer to the enclosed FASTCOM CD for example programs, product updates, and software for testing your installation. Refer to the [Infineon PEB 20534 User's Manual](#) for register information.

Local Bus Interface for PEB 20534

Byte accesses: refer to the readlb.c and writelb.c example programs.

Register at offset 0 - No function

Register at offset 1 - No function

Register at offset 2

<p>Channel 1</p> <p>Bit 0 0 = ST connected to TXCLK 1 = ST not connected</p> <p>Bit 1 0 = TT connected to TXCLK 1 = TT not connected</p> <p>Channel 2</p> <p>Bit 2 0 = ST connected to TXCLK 1 = ST not connected</p> <p>Bit 3 0 = TT connected to TXCLK 1 = TT not connected</p>	<p>Channel 3</p> <p>Bit 4 0 = ST connected to TXCLK 1 = ST not connected</p> <p>Bit 5 0 = TT connected to TXCLK 1 = TT not connected</p> <p>Channel 4</p> <p>Bit 6 0 = ST connected to TXCLK 1 = ST not connected</p> <p>Bit 7 0 = TT connected to TXCLK 1 = TT not connected</p>
---	---

Register at offset 3

<p>Channel 1</p> <p>Bit 0 0 = RT normal 1 = RT inverted</p> <p>Bit 1 0 = TT normal 1 = TT inverted</p> <p>Bit 2 0 = ST normal 1 = ST inverted</p> <p>Bit 3 No function</p>	<p>Channel 2</p> <p>Bit 4 0 = RT normal 1 = RT inverted</p> <p>Bit 5 0 = TT normal 1 = TT inverted</p> <p>Bit 6 0 = ST normal 1 = ST inverted</p> <p>Bit 7 No function</p>
---	---

Register at offset 4

<p>Channel 3</p> <p>Bit 0 0 = RT normal 1 = RT inverted</p> <p>Bit 1 0 = TT normal 1 = TT inverted</p> <p>Bit 2 0 = ST normal 1 = ST inverted</p> <p>Bit 3 No function</p>	<p>Channel 4</p> <p>Bit 4 0 = RT normal 1 = RT inverted</p> <p>Bit 5 0 = TT normal 1 = TT inverted</p> <p>Bit 6 0 = ST normal 1 = ST inverted</p> <p>Bit 7 No function</p>
---	---

Offset 2 – These bits are for setting the transmit clock direction. The PEB20534 has only one transmit clock pin that can be an input or an output using CCR0:TOE. If that pin is configured to be an output, then it must be

connected to a line driver. If that pin is configured to be an input, then it must be connected to a line receiver. The ST pin is TxClk as an input and the TT pin is TxClk as an output.

- ST connected to TxClk – TxClk connected to the ST input pin. **Never set CCR0:TOE=1 when setting this bit!**
- ST not connected to TxClk – (default) TxClk not connected to the ST input pin
- TT connected to TxClk – (default) TxClk connected to the TT output pin
- TT not connected to TxClk – TxClk not connected to the TT output pin.

Note: It is possible to configure the TxClk pin as an input TOE=0, and connect it to both the TT and ST pins. This will allow the external clock from the ST pins to be outputted on the TT pins.

Offset 3 & 4 – We have designed this board so that it is configurable to meet your platform's RS-232 needs. Some users will discover that their clock signals are inverted in relation to the signals coming off of the SuperFastcom card. In that case, we provide these registers to modify our signals to match theirs.

- RT normal – (default) Our default receive clock setting
- RT inverted – Invert the receive clock
- TT normal – (default) Our default transmit clock output setting
- TT inverted – Invert the transmit clock output
- ST normal – (default) Our default transmit clock input setting
- ST inverted – Invert transmit clock input

MEMORY MANAGEMENT

High-speed communications requires that large amounts of transmitted/received data be buffered so as to prevent data loss and maintain data throughput. The *SuperFASTCOM 232/4-PCI* is designed to utilize system memory directly, bypassing the system processor. The *SuperFASTCOM 232/4-PCI* accesses system memory through high-speed PCI Bus Mastering, using its on-board bus master controller and supplied software. This procedure for direct memory access (DMA) is by far the fastest, most efficient method of handling the large amounts of data that high-speed communications generates. Data is transferred to and from the *SuperFASTCOM 232/4-PCI* adapter at data bus speed. Buffering a high-speed data stream is critical in order to maintain data integrity and reliability, to avoid data loss, and to prevent data overrun. The *SuperFASTCOM 232/4-PCI* does all this with minimal system processor involvement; therefore, there is no reduction in processor performance due to data communication overhead.

How it works - The user designates in his program how much system memory will be allocated to communications -- the more memory in your system, the more you can allocate to the communication process. As data is received, the on-board communication processor fills a small local buffer. When this is full, the bus master controller on the *SuperFASTCOM 232/4-PCI* transfers this data directly to system memory. The local buffer is reset and the process begins again. Transmitting data works in reverse; data from system memory is directly transferred to the local buffer on the *SuperFASTCOM 232/4-PCI*. When the local buffer is empty, new data from memory is directly transferred in. All of this occurs without slowing or interfering with the system processor.

The high speed PCI Bus Mastering procedure for direct memory access provides the fastest, most efficient method of data transfer. It also improves efficiency and reduces the cost of the *SuperFASTCOM 232/4-PCI* board by eliminating the need for on-board memory or a processor.

MAXIMUM DATA RATE

Due to the nature of RS-232 communications, attainable baud rates tend to vary greatly. The ability to achieve higher baud rates depend on many factors including the interrupt handling ability of target machine, environment noise and especially cable lengths.

In order to make cable length determination easier, we have developed an equation based on an interpolation of recorded laboratory data. By measuring the maximum attainable baud rates at varying cable lengths and plotting the data, we were able to create a linear approximation of the data set.

Please use the equation below to determine approximate correlations between maximum baud rate and cable length up to a typical maximum of 2,062,500 bps (rates above 1 Mbps are possible but not guaranteed).

- To determine the max length at a given baud use:

$$d = (-9.04 \times 10^{-5} * \text{bps}) + 192$$

- To determine the max baud at a given cable length use:

$$\text{bps} = (-11,000 * d) + 2.13 \times 10^5$$

d = approximate MAX cable length in feet

bps = estimated MAX baud rate in bits per second

Equations are based on experiments using Olympic cable number 2829 with 30pf/ft nominal capacitance at a maximum of 83 ft (CL not to exceed 2500 picofarads per EIA-232). These equations are an estimate of the maximum capabilities in users' environments; different cable capacitance will yield different results. These equations are only valid when using a *SuperFASTCOM* 232/4-PCI adapter, they cannot be utilized when dealing with other Fastcom boards.

ERRATA

The errata listed below are known issues with the either Superfastcom board or the PEB20534 controller itself. For more information regarding any of these issues, please contact Commtech [technical support](#).

- **Serial Bus Configuration Timing Modes**

The SuperFastcom was not designed to make use of Serial Bus Configuration timing modes 1 and 2. Do not attempt to configure CCR0:SC(2..0) to use these modes as they will not work correctly.

- **Maximum Value of Baudrate Generator**

The maximum value 'BRM' in register BRR must not exceed $M = 14$ (the specified maximum value is $M = 15$). This limits the baud rate generator unit to frequency division factors in the range $k = 1 \dots 1,048,576$, instead of $k = 1 \dots 2,097,152$.

- **DPLL Algorithm for FM0, FM1 and Manchester Encoding**

Recovering the clock from an FM0-, FM1- or Manchester-encoded receive data stream using the DPLL circuitry is not working. The DPLL-asynchronous interrupt (PLLA) occurs continuously.

- **HDLC Mode: False Receive Status Byte**

The receive status byte RSTA belonging to an already received frame is overwritten by 0x00 if the following two conditions are met:

1. The interframe timefill number of '1' bits between the closing flag and the opening flag of the next frame is in the range of [1 - 5].
2. The receive CRC checking mode is selected to transfer the receive CRC into the receive FIFO (CCR2:RCRC = '1').

In all cases meeting the first condition, the number of '1' bits is treated as an invalid HDLC frame. This frame is prevented from being reported or forwarded to the receive FIFO because of its invalid length. However the serial receive logic calculates a receive status byte RSTA = 0x00 (invalid frame).

If the receive CRC is selected to be transferred to the receive FIFO (second condition), the receive status value of the previous valid frame is not yet transferred when calculating the invalid receive status byte. Thus the original receive status value is overwritten by 0x00 marking the previous frame as 'invalid'.

Workaround: The error cannot occur if bit CCR2:RCRC is set to '0', i.e. receive CRC is not transferred to the receive FIFO. Otherwise (if CCR2:RCRC = '1') reception of less than 6 consecutive '1' bits as interframe timefill must be avoided. This can be achieved by the transmitter either selecting interframe timefill flag sequences or preamble transmission.

- **HDLC Mode: Transmission with Shared Flags**

If the shared flag option is enabled in HDLC mode via bit CCR1:SFLAG, the first byte of a frame might be replaced by a '7E' flag or 'FF' octet on the transmit line, depending on the interframe time fill selection (bit CCR2:ITF). This leads to a damaged transmit frame.

Workaround: It is recommended to disable shared flag transmission by setting bit CCR1:SFLAG = '0'.

Note: Reception of frames with shared flags is always possible and neither affected by this erratum nor by setting of bit CCR1:SFLAG. Thus networking with other HDLC equipment supporting shared flags is not restricted.

- **Asynchronous PPP Mode: Reception**

In asynchronous PPP mode the SCC receiver expects a back-to-back stream of ASYNC characters. Once synchronized on the first ASYNC character the receiver expects further octets back-to-back in a fixed scheme determined by the (8, N, 1) character format. The receiver does not synchronize again on subsequent ASYNC characters.

Workaround: Do not attempt to configure ASYNC PPP mode, to realize asynchronous PPP mode it is recommended to configure the SCC in ASYNC mode, implementing CRC calculation and character mapping in software. Examples for fast CRC calculation and the character mapping specification are given in RFC 1662 (July 1994) document.

- **Extended Transparent Mode: Minimum Frame Length**

If the frame length in extended transparent mode is programmed to one, an XDU interrupt is generated with all its consequences (transmit SCC stops).

Workaround: Frame lengths of 2 or more bytes should be used instead. If a 1-byte frame shall be sent, an idle character should be attached to it.

- **HDLC Automode: Full-duplex Operation**

In HDLC Automode the transmission of an I-frame might be spoiled by simultaneous reception of a frame, sometimes resulting in endless repetition of a byte or in failure of the responding S-frame. Then this channel does not respond autonomously to further reception events.

Workaround: None. Do not use full-duplex Automode.

- **Command Execution (CEC) Status Bit Error With External Clocking**

In general the PEB20534 supports external clock gapping in any clock mode in which the internal transmit or receive clock is supplied via the dedicated RxClk and/or TxClk pins. If one of the clocks is externally gapped, the respective receive or transmit block remains in its current static condition until the clock signal is active again. Any command bit in register CMDR (e.g. 'XRES' and 'RRES') effects either the transmit or receive logic and command execution only depends on this block and its clock supply respectively. Nevertheless all commands are forwarded to both transmit and receive block and command execution must be reported internally by both blocks to reset status bit STAR:CEC. Another command is only accepted if 'CEC' bit is cleared.

Example: The SCC is configured in clock mode 0a, a clock signal is provided at pin TxClk but pin RxClk is supplied with a constant value (no clock signal or gapped). A transmitter reset command applied by write access to register CMDR will be executed by the transmit block, but status bit 'CEC' remains active afterwards, because the receive block cannot report command execution without clock supply. Any further command will be ignored while 'CEC' bit is active.

Workaround: Transmit and receive blocks must be supplied with clock signals in general. Because reset of the command execution (CEC) status bit might be delayed due to one of the clocks temporarily gapped, 'CEC' status bit must be checked for '0' before writing a command bit.

- **Carrier Auto-detect in HDLC Mode**

The carrier detect (CD) input pin is supposed to enable and disable reception in clock modes 0, 2, 3, 6 and 7. In HDLC/PPP mode this function is not working properly and thus should not be enabled with bit CCR1:CAS.

- **Receiver in Extended Transparent Mode Does Not Initialize**

When attempting to use Extended Transparent Mode (raw bits), it appears as though the receiver does not activate. It unclear whether this is a bug in the PEB20534 or whether it was done by design, but the port that will be receiving in Ext. Trans. Mode must be initialized in clock mode 1 with a clock present on the RT pins. It can then be switched to any other clock mode and will operate correctly.

Workaround: If your configuration already uses an external receive clock, simply initialize the card in clock mode 1 (CCR0:CM2..CM0 = '001') with a clock present on the RT pins and then change to whatever clock mode you wish to use. If you do not have an external clock, you can utilize the PROGCLK output pins that are located on the DB25 connector for port 1 at pins 20 and 23. Jumper the PROGCLK pins to the RT pins of your receiving port and initialize the card in clock mode 1.

TECHNICAL SUPPORT

Commtech provides extensive technical support and application suggestions. Most of the problems that occur with the *SuperFASTCOM 232/4-PCI* can be corrected by double-checking the switch positions, your cables and your program. We recommend that you build the loop back plug that is described in the Programming section of this manual. With that plug, you can quickly isolate the problem to the board, cables, or software.

If you still have unresolved questions, use the following procedure to get technical support:

1. Call our Technical Support Staff at (316) 636-1131. They are on duty from 9:00 AM to 5:00 PM Central Time.
2. Ask for technical support for the *SuperFASTCOM 232/4-PCI*. Be ready to describe the problem, your computer system, your application, and your software.
3. If necessary, our staff will give you an RMA number (Return Material Authorization). Use this number on the mailing label and in all references to your board. Put the board back in its static bag and in its box. Ship the board back to us as directed.
4. If you prefer, you may FAX a description of the problem to us at (316) 636-1163, or we can be reached on the Internet at "<http://www.commtech-fastcom.com/TechSupport.html>" or by email at "techsupport@commtech-fastcom.com".

FASTCOM LIMITED LIFETIME WARRANTY

Commtech's entire FASTCOM product line is covered by a limited lifetime warranty against defects in workmanship. This warranty is available only to the original purchaser and only covers defects in our workmanship. Any FASTCOM board that is returned to Commtech will, at the option of Commtech, be repaired or replaced at no charge -- except for circumstances excluded by this warranty.

A Return Materials Authorization (RMA) number must be obtained from Commtech before a return will be accepted. Please contact us via telephone or email to obtain an RMA number.

You are responsible for shipping charges when you return a FASTCOM board to Commtech. We will pay the shipping charges to send the board back to you if a defect in workmanship is found. However, if no defect in workmanship is found, or the board is not found to be defective, or the any of the following warranty exclusions occur, you will be responsible for shipping charges both ways.

Warranty Exclusions

This warranty does not cover problems or damage resulting from, but not limited to, the following:

1. Any modification, misuse, abuse, disassembly, misapplication, or unauthorized repair by anyone other than Commtech.
2. Any improper operation, including any use not in accordance with any verbal product instructions or documentation.
3. Connection to an improper voltage supply or ESD damage.
4. Any other cause not related to workmanship.

Non-Warranty Repairs

We can provide a quote for non-warranty repairs upon request.

If any Commtech product is damaged such that it cannot be repaired, you can return it to Commtech for replacement under our *Non-Repairable Replacement* policy, regardless of the cause of damage. Commtech will replace the unit at 60% of the then-current list price.

Limitation of Liability

Commtech shall not be liable for any special, incidental, indirect, or consequential damages whatsoever, including but not limited to loss of profits, revenue, or data (whether direct or indirect), or commercial loss for breach of any express or implied warranty on your product even if Commtech has been advised previously of the possibility of such damages. Commtech's liability, in any case, shall not exceed the original product purchase price.

APPENDIX A

INFINEON 20534

TECHNICAL DATA

